

CM-iVCF Computer-On-Module

Reference Guide

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1. Revision Notes

Date	Description
10-Apr-2005	Preliminary release
19-Apr-2005	Local Bus specifications updated
29-Aug-2005	Added missing PCI-INTC, PCI-INTD
19-Nov-2005	Added clarifications about heatsink cooling requirements
18-Jun-2006	Modified to reflect transition to C7 / CN700 chipset, due to C3 discontinuation.

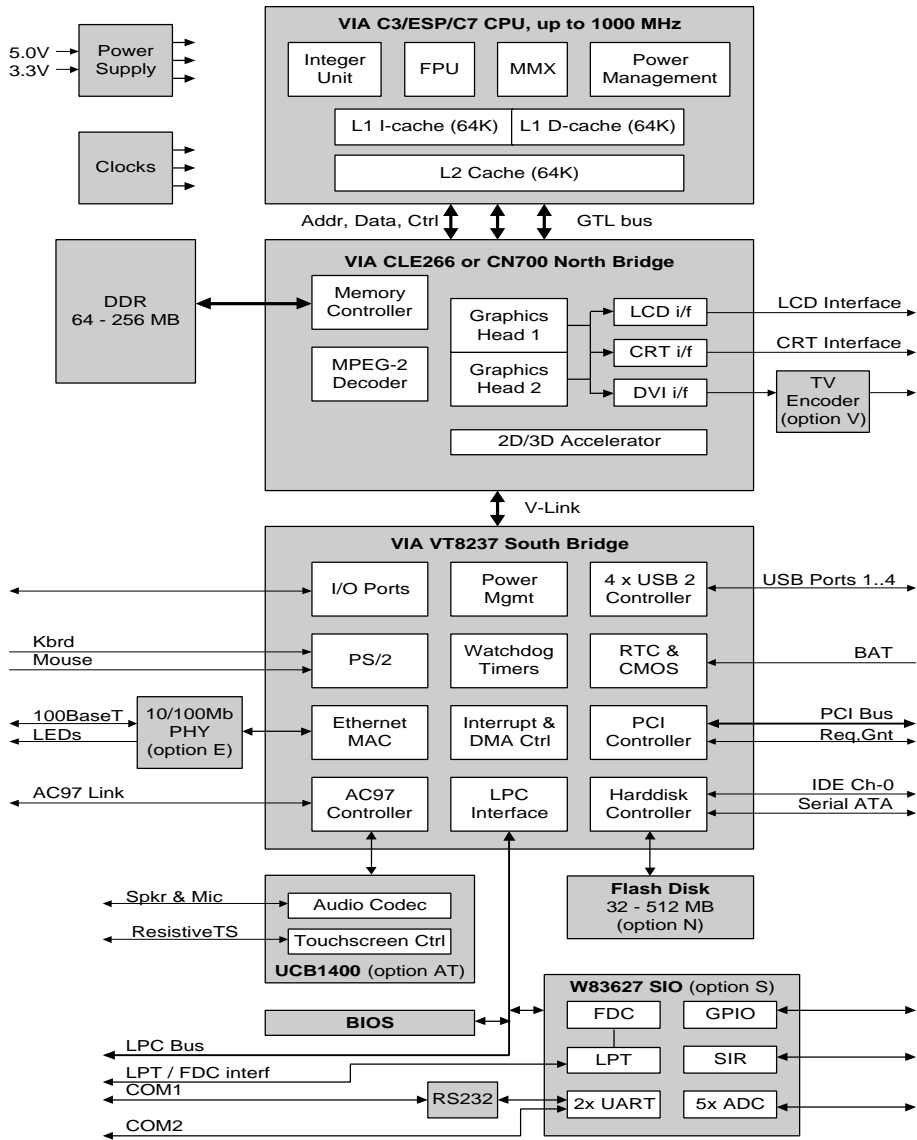
Please check for a newer revision of this manual in CompuLab's website - <http://www.compulab.co.il>, following [Developer] >> [iVCF] links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

2. Overview

2.1. Highlights

<ul style="list-style-type: none">▪ Full-featured high performance embedded PC on module▪ VIA X86 CPU architecture using C3 or C7 processor, up to 1000 MHz▪ PCI, LPC and AC97 buses▪ 64 - 256 Mbyte DDR▪ 16 - 512 Mbyte Flash Disk▪ Dual Head SXGA graphics controller for LCD, CRT and TV▪ MPEG Decoder▪ Video Input Port▪ Four USB 2 ports▪ UART's, LPT port, GPIO's, hard and floppy disk controllers, PS/2 keyboard and mouse ports▪ 10/100BaseT Ethernet▪ Sound I/O and Touchscreen support▪ Embedded BIOS▪ Small size - 70 x 86 mm▪ Interchangeable with other CoM's via CAMI connectors▪ Mini-ATX baseboard for evaluation and development	<p>The CM-iVCF module is a small but extremely powerful PC-compatible Computer-On-Module, designed to serve as a building block in a variety of embedded applications. The CM-iVCF has all the components needed to run operating systems such as Windows XP, Windows CE or Linux. Ready BIOS and operating systems packages are available from CompuLab.</p> <p>The CM-iVCF is both small and inexpensive relative to products of its class, which allows its integration into compact applications requiring both embedded and multimedia feature sets.</p> <p>The feature set of the CM-iVCF module includes practically all of the components found in a high-end desktop computer. For embedded applications, the CM-iVCF provides a Flash Disk, PCI bus, 100Mbit Ethernet, UART's, I/O lines and many other essential functions. For multimedia applications, the CM-iVCF has a dual head graphics controller, an MPEG decoder, video input, sound and touchscreen controllers.</p>
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2.2. Block Diagram



2.2

2.3. Features

The "Option" column specifies the P/N code required to have the particular feature. "+" indicates that the feature is always available.

CPU & Core logic

Feature	Specifications	Option
CPU	VIA CPU architecture, using either C3 or ESP or C7 processor packing, X86/Pentium compatible, up to 1000 MHz	C
Internal Bus	64-bit, 133 MHz	+
Cache	64 + 64 KB L1 and 64 KB L2 Cache	+
Core Logic	DMA and Interrupt controllers, Timers	+

Memory and Busses

Feature	Specifications	Option
DRAM	64 - 256 MB DDR, 266 MHz, 64-bit	D
BIOS Flash	1/2 Mbyte, on-board reprogrammable	+
NAND Flash Disk	32 - 512 Mbytes	N
External Busses	PCI, LPC, AC97 and simple Local Bus	+
AC97	AC97 / AMC97 Rev 2.1 compliant	+
PCI bus	32-bit, rev 2.2-compliant, 132 MB/s, 5-volt tolerant Arbiter and clock for 4 masters	+
LPC bus	Host, 33 MHz, Intel LPC v1.0 compatible	+

Peripherals

Feature	Specifications	Option
Graphics Controller	Dual head, resolution up to 1600 x 1200, 16-64 MB frame buffer in system memory, 2D/3D hardware accelerator.	+
Display Interface	LCD - 18-bit TFT (parallel RGB)	+
	CRT - 24-bit resolution (analog RGB), 250 MHz RAMDAC	+
	TV - on-board VT1622A encoder, PAL / NTSC	V
MPEG-2 Decoder	Full speed DVD playback	+
USB	Four Host USB 2.0 ports, 480 Mbps, EHCI / UHCI compliant	+
UART's	Two UART's, including flow control	S
GPIO	10 lines from chipset plus 13 lines from Super-I/O	+

CM-iVCF Embedded PC Module

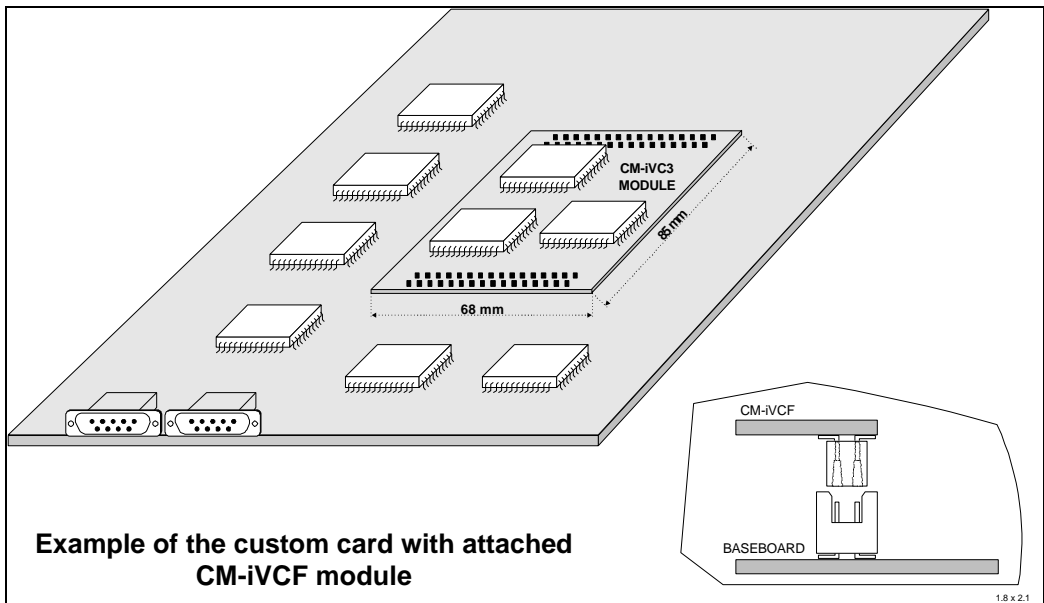
Hard Disk Interf.	IDE and S-ATA interf., UDMA-133 mode, 70 MB/s transfer rate	+
LPT - Parallel Port	Bi-directional with EPP mode.	S
Floppy Disk Interf.	Routed through LPT pins	S
Kbrd & Mouse	PS/2 or USB or redirection from serial port	+
Infrared (IrDA)	Up to 115Kbps in SIR mode	S
Ethernet	MAC & PHY, 10/100BaseT, Activity LED's.	E
Audio codec	Phillips UCB1400, AC97 interface, mono microphone input, stereo line input and 25 mW output for active speakers	AT
Touchscreen ctrl.	A part of the UCB1400 codec chip. Supports resistive touch panels.	AT
RTC	Real Time Clock, powered by external lithium battery	+
Analog inputs	5 channels, 8-bit	S
Hardware monitoring	Optional monitoring of CPU temperature and CPU power supply voltage	S

Electrical, Mechanical and Environmental Specifications

Supply Voltage	3.3V and 5.0V
Power	8 - 12 watt, depending on configuration and CPU speed
Dimensions	70 x 86 mm. Height: 21 mm w/heatsink or 10 mm w/o heatsink
Weight	60 gram w/o heatsink, 130 gram with heatsink
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C Extended: -20° to 70° C Industrial: -40° to 85° C Note: user must assure that heatsink temperature would not exceed allowed maximum. In still air heatsink temperature can rise up to 50°C above ambient. Heatsink should be cooled by airflow or heat extruders.
Storage temp.	-40° to 85° C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	3 x 140 pin, 0.6 mm. Insertion removal - up to 50 cycles

2.4. General Description

The CM-iVCF is a miniature single board computer packed as a module. It contains a CPU, memory, flash disk and peripherals. All interface functions of the CM-iVCF are routed through miniature high-density connectors, designed for piggyback attachment to a custom baseboard, as shown in the picture below.



2.5. VIA "Nehemiah" CPU Architecture

Nehemiah architecture has 16-stage integer pipeline. At basic level, it is divided into four major functional groups: I-fetch, decode and translate, execution, and data cache.

The *I-fetch* components deliver x86 instruction bytes from the large I-Cache or from the external bus. Large buffers allow fetching to proceed asynchronously to other operations. The *decode and translate* components convert x86 instruction bytes into internal execution forms. Branches are also identified, predicted, and the targets pre-fetched. The *execution* components issue, execute, and retire internal instructions. The *data cache* components manage the efficient loading and storing of execution data to and from the caches, bus, and internal components.

VIA Nehemiah processor architecture is relatively simple - instructions are issued, executed, and retired in order, one instruction is issued per clock. On the other hand, the design is highly optimized to achieve high performance in the targeted environment. Some of the significant features providing this performance are:

High internal clock frequency:

- The 16-stage pipeline facilitates high MHz

Large on-chip caches and TLBs:

The VIA Nehemiah CPU implements large caches and TLBs that significantly reduce stalls due to bus traffic:

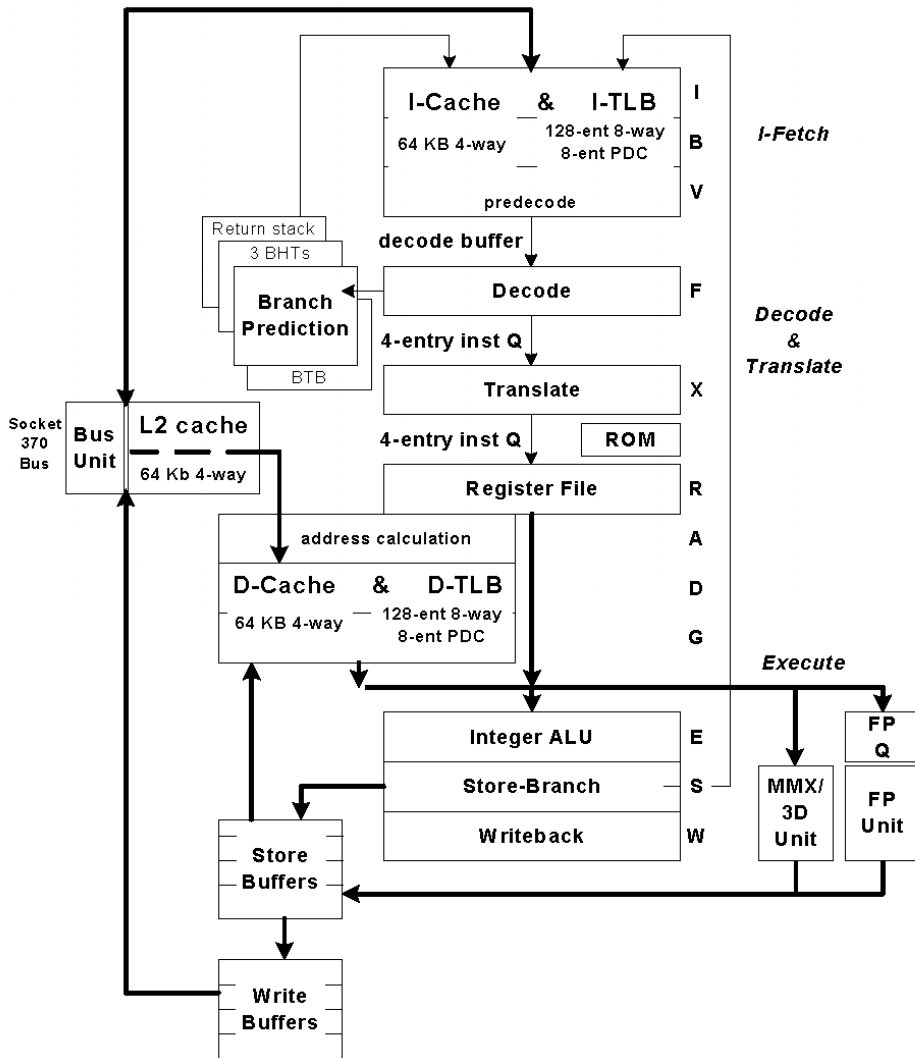
- Two 64-KB primary (L1) caches with 4-way associativity
- A 16-way 64-KB unified level-2 (L2) cache
- Two 128-entry TLBs with 8-way associativity
- Two 8-entry page directory caches that effectively eliminate loads of page directory entries upon TLB misses
- A four-entry (8 bytes each) store queue that also forwards store data to subsequent loads
- A four-entry write buffer that also performs write combining

Extensive features to minimize bus stalls:

- Full memory type range registers (MTRRs)
- A non-stalling write-allocate implementation
- Implementation of the "cache lock" feature
- Non-blocking out-of-order retirement of pipeline stores
- Implementation of x86 prefetch instruction (3DNow!)
- Implicit speculative *data* prefetch into D-cache

- Implicit instruction prefetch into I-cache
- Asynchronous execution with extensive queuing to allow fetching, decoding and translating, executing, and data movement to proceed in parallel

VIA "Nehemiah" Architecture Block Diagram



X86 architecture CPU's are available from VIA in processor product lines named C3, ESP and C7. Earlier versions of CM-iVCF module are using ESP processor, later version will use C7. There is no functional difference between different members of VIA's X86 CPU architecture.

2.6. Flash Disk

One of the key advantages of CM-iVCF architecture is its on-board flash disk, supported by all operating systems available for the CM-iVCF. The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts and it is built into the CM-iVCF module.

NAND Flash provides storage solution for embedded applications requiring large, non-volatile on-board storage. The NAND Flash is a block device - optimized for block read and write operations rather than for random access. The NAND Flash Driver, integrated in BIOS and O/S kernels, implements standard hard disk functionality. The NAND Flash is available from 16 to 512 Mbytes. The CM-iVCF is designed for upward compatibility with future NAND Flash devices of larger capacity.

Flash Disk Driver

The Flash Disk Driver emulates disk-like behavior using the Flash memory component. The driver's code is operating system independent - the same code is used for all operating systems. However, since each operating system requires that the driver be integrated through a different interface, CompuLab provides a Flash Disk Driver kit per operating system. Driver code is also included in BIOS, to provide Flash Disk service for operating systems accessing the disk through BIOS calls. The driver performs the following functions:

- Translation of sector read/write requests coming from the operating system to block access operations on physical media (Flash)
- Buffering and consolidation of sector write operations
- Mapping and swapping-out of bad blocks
- Error correction using ECC
- Anti-wearing
- Crash / power fail protection

Anti-wearing algorithm

The Flash Disk Driver ensures that block write operations will be distributed evenly across the physical media, regardless of the location (logical sector number) requested by the operating system. Even distribution assures that all Flash blocks will be worn at the same (slow) rate and the Flash will continue operating for a long time without reliability degradation. The following example outlines expected reliability.

Flash actual data: Size - 16 MB. Guaranteed minimum of writes per block - 1,000,000.

Assuming that a specific application continuously writes to the Flash Disk, 300KB per minute then:

Guaranteed life time = $[16\text{MB} * 1,000,000] / 300\text{KB}/\text{min} = 101 \text{ years (!)}$

This example shows that the guaranteed period of reliable operation is well above any practical limit.

Reliability

The reliability issue concerns two different aspects: mechanical and functional.

Mechanical reliability of the Flash Disk is far above that of its hard disk counterpart, as it doesn't have any moving parts and is securely soldered on-board.

In terms of functional reliability, the Flash Disk is similar to a standard, high-quality Hard Disk. Operating systems using the Flash Disk will perform with the same or better reliability level than that of its hard disk counterpart.

Fault Tolerance

Flash Disk Driver algorithms and data structures are designed for full recovery in the event of an operating system crash or unexpected power off. The Driver achieves fault tolerance through the following method:

When new data is stored and control information should be updated, the driver first copies the control information to a new location and alters it accordingly. When control information is finally updated, the driver switches between the old and new copies in a single step. Only then is the previous copy is deleted.

If driver operation is aborted in the middle, due to power off for example, on the next start, the driver will use the last valid copy of control information and will remove the newer, incomplete copy.

The fault tolerance implemented by the Flash Disk Driver ensures that its operation will remain correct and consistent, i.e., it will continue emulating hard disk behavior. It doesn't however provide any remedy for an incorrect state of a file system, which may be caused by the operating system itself in the event of a crash. Problems like these are transparent to the Flash Disk Driver and should be handled on the operating system level. For example, Linux files can be protected against power fails by using EXT3 file system with journaling.

Performance

Read	1000 KB/s
Write	600 KB/s

The Flash Disk has an internal write buffer. The buffer's contents are flushed into non-volatile media within 200 ms after write operation. Therefore, the requirement for a 200 ms delay should be taken into account when scheduling system shutdown.

Write Protection

For extended reliability, two methods of write protection are provided:

1. Hardware level: WP2# input on module interface completely prevents flash write and erase operations.
2. Driver level: user can specify one protected region for which the driver will prevent write and erase operation. This allows protection of specific partition containing critical code, while rest of the flash disk can be used in regular read/write manner.

Note: another input - WP1# protects BIOS flash, including code and settings.

3. Peripherals and Functions

Interrupt Channel Mapping

IRQ	I/O Device	Priority	On-board usage
IRQ0	PIT 0	P1	always
IRQ1	Keyboard interface	P2	SIO
IRQ2	Slave controller cascading	—	always
IRQ3	COM B, off-board PCMCIA	P11	SIO
IRQ4	COM A, off-board PCMCIA	P12	always
IRQ5	PCI	P13	-
IRQ6	Floppy disk controller	P2	SIO
IRQ7	Parallel port, off-board PCMCIA	P22	SIO
IRQ8	Real-time clock	P3	always
IRQ9	PCI	P4	-
IRQ10	PCI	P5	-
IRQ11	PCI	P6	-
IRQ12	Mouse interface	P7	SIO
IRQ13	Floating point error	P8	always
IRQ14	IDE	P9	-
IRQ15	Serial ATA / NAND Flash / Off-board PCMCIA	P10	NAND Flash

If IRQ used by on-board device, disabling the device will free the IRQ. If on-board device cannot be disabled, than IRQ is *always* assigned for the on-board usage and therefore marked so in the table above. PCI interrupts support interrupt sharing, therefore same interrupt may be used by several devices (on-board and off-board).

Options of IRQ assignment for external use

Signal	Pin	Initial mapping by BIOS	On-board usage
GPIRQ0	P1-51	Can be assigned to IRQ 3,4,6,7. Disabled by default. See reference code.	
IDE-IRQ	P1-49	IRQ14	None / IDE on ATX baseboard
GPIRQ1	P1-54	IRQ15	NAND flash

* IRQ inputs are available for external usage only when not used by an on-board function.

Serial IRQ

The CM-iVCF provides another interface for interrupt requests – serial IRQ. This allows a single signal line to be used to report the legacy ISA interrupt requests. Interrupt sharing is allowed on Serial IRQ interfaces only for the devices external to chipset. The following interrupts are external to chipset and therefore potentially available on the Serial IRQ interface: IRQ3, IRQ4, IRQ6, IRQ7. The serial IRQ interface is a synchronous interface. Data is clocked by the system's PCI clock.

Serial IRQ interface

Signal	Pin	Type	Description
SERIRQ	P2-13	I/O	The routing for this signal must be done using PCI layout/routing rules.

3.1. Watchdog

Watchdog is available in VT8237 south bridge. Timer has 8-bit counter that counts down the 1 sec clock ticks. The counter is loaded with initial value and counts down. On reaching zero the first time it is automatically reloaded with original value. On reaching zero the second time it generates system reset. The timer status can be read at any time and can be updated at any time. Watchdog can be de-activated by disabling the timer clock source. Driver and demo for watchdog operation is provided in O/S packages.

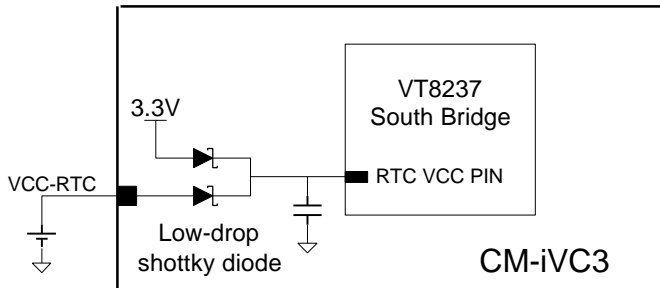
3.2. Real-Time Clock

The RTC is compatible with the standard used in PC/AT systems. The RTC consists of a time-of-day clock with an alarm interrupt and a 100-year calendar. The clock / calendar has a programmable periodic interrupt, 242 bytes of static user RAM, and can be represented in either binary or BCD. The RTC includes the following features:

- Counting of seconds, minutes, and hours of the day
- Counting of days of the week, date, month, and year
- 12–24 hour clock with am and pm indication in 12-hour mode
- 242 bytes of general-purpose RAM
- Three separate software-maskable and testable interrupts: (1) Time-of-day alarm is programmable to occur from once-per-second to once-per-month, (2) Periodic interrupts can be configured to occur at rates from 122 ms to 500 ms, (3) Update-ended interrupt provides cycle status
- The voltage monitor circuit checks the voltage level of the backup lithium battery and sets a bit when the battery voltage level falls below specification.

- Internal RTC reset signal performs a reset when power is applied to the RTC core.

The RTC uses a dedicated lithium backup battery when the rest of the card is completely powered down (RTC-only mode). The RTC can continue operating even when the rest of the card is not powered. The battery should be connected to the VCC-RTC (V_{BAT}) input of the CM-iVCF's interface connector. The equivalent RTC supply circuit is shown in the figure below.



	Typical	Max
RTC-VCC Input Current (Rest of the card powered down)	2 μ A	5 μ A

Storing of BIOS Settings

The CM-iVCF's BIOS has two sets of stored settings:

- Current settings stored in CMOS memory, backed-up by battery as described above. The battery is not located on the CM-iVCF itself, but rather should be provided on the baseboard. When CMOS is not powered, the settings it saves are lost.
- Default settings saved in Flash memory. These settings remain valid when the card is not powered, even in the absence of battery backup. The user can update the Flash default settings to any desired values.

On startup, BIOS checks if valid CMOS settings are available. If they are, BIOS takes the settings from CMOS. Flash defaults are ignored in that case. If CMOS settings are not valid (i.e., were erased), BIOS uses the default settings from Flash. In this case, BIOS also copies the default settings from Flash to CMOS, to make it valid.

3.3. Display Controller

The powerful Display Controller of CM-iVCF contains comprehensive set of features required for multimedia applications:

Integrated Graphics / Video Accelerator

- Optimized Shared Memory Architecture (SMA)
- 8 / 16 / 32 / 64MB frame buffer using system memory
- Internal AGP 4x-equivalent performance
- Separate 128-bit data paths between North Bridge and graphics core for pixel data flow and texture / command access
- Graphics engine clocks up to 133 MHz decoupled from memory clock
- High quality DVD video playback
- VIP 1.1 / VIP 2.0-compatible video capture inputs up to 165 MHz data rate
- Internal hardware VGA controller with true-color / high-color sprite for hardware cursor implementation
- 128-bit 2D and 3D graphics engines
- Floating point triangle setup engine
- 3M triangles/second setup engine
- 133M pixels/second trilinear fill rate

Extensive Display Support

- CRT display interface with 24-bit true-color RAMDAC up to 250 MHz pixel rate with gamma correction capability
- Direct TFT flat panel interface up to 18-bit data width
- 12-bit DVI and TV Encoder for NTSC or PAL TV display
- Support for panel resolutions up to 1600x1200, CRT resolutions up to 1400x1050
- Automatic panel power sequencing and VESA DPMS CRT power-down
- Dual view capability where CRT and Flat Panel Monitor or TV output can have a different picture, resolution and refresh rate

Video Support

- Up to three video windows for video conferencing applications
- High quality scaler (up or down) for both horizontal and vertical scaling. Linear interpolation for horizontal and vertical up-scaling and filtering for horizontal and vertical down-scaling.
- Color space conversion
- Color enhancement (contrast, hue, saturation, brightness and gamma correction)
- Color and chroma key support
- Hardware sub-picture blending
- Bob / weave de-interlacing mode and advanced de-interlacing to improve video quality

- Video capture inputs with built-in phase adjuster to fine tune the clock/data signal timing
- Supports CCIR601 standard

MPEG-2/1 Video Decoder

- Motion compensation for full speed DVD playback
- Hardware accelerated Slice layer, IDCT and Motion compensation

2D Hardware Acceleration Features

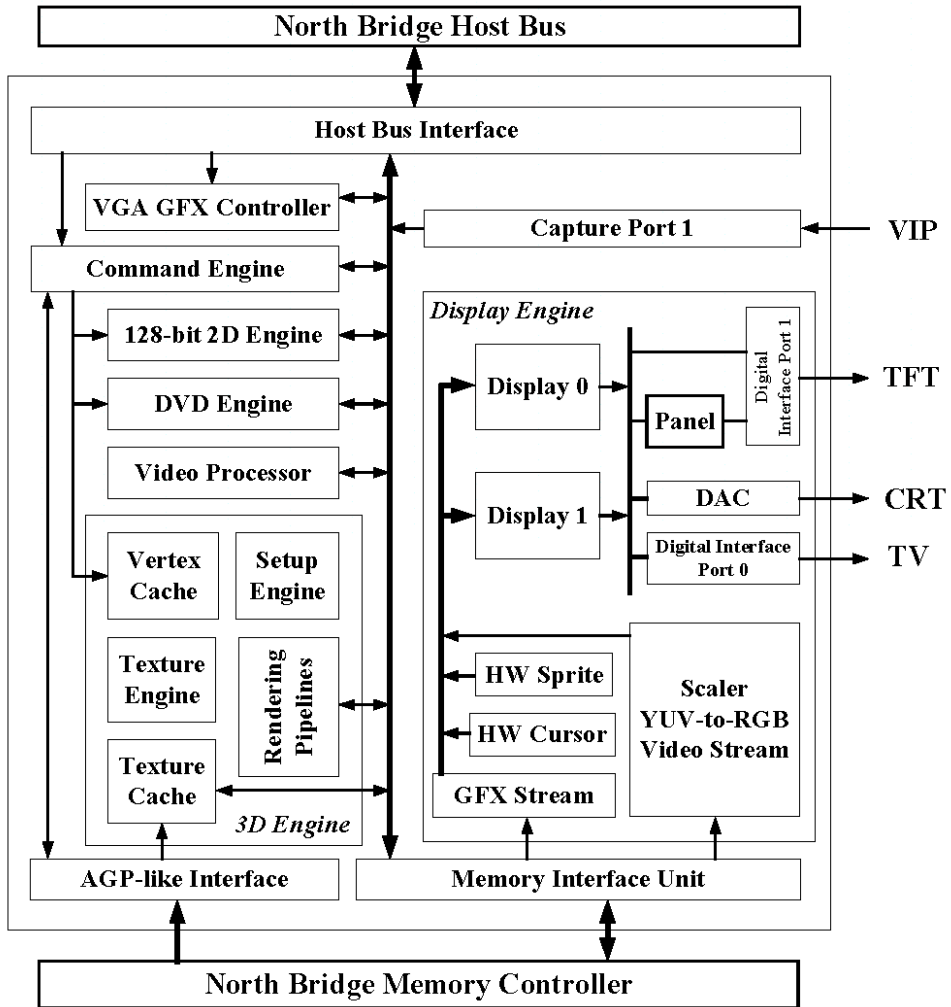
- BitBLT (bit block transfer) functions including alpha blts
- Text function
- Bresenham line drawing / style line function
- ROP3, 256 operation
- Color expansion
- Source and destination color keys
- Transparency mode
- Window clipping
- 8, 15/16 and 32 bpp mode acceleration

3D Hardware Acceleration Features

- Microsoft DirectX 7.0 and 8.0 compatible
- OpenGL driver available
- Floating-point setup engine
- Triangle rate up to 3-million triangles per second and Pixel rate up to 133-million pixels per second for 2 texture, depth test and alpha blending
- Flat and Gouraud shading
- Hardware back-face culling
- 16-bit, 32-bit Z test and 24+8 Z+Stencil test support
- Z-Bias support
- Stipple Test, Line-Pattern test, Texture-Transparence test, Alpha test support
- Edge anti-aliasing support
- Two textures per pass
- Tremendous Texture Format: 16/32 bpp ARGB, 1/2/4/8 bpp Luminance, 1/2/4/8 bpp Intensity, 1/2/4/8 bpp Paletized (ARGB), YUV 422/420 format
- Texture sizes up to 2048x2048
- High quality texture filter modes: Nearest, Linear, Bi-linear, Tri-linear, Anisotropic
- LOD-Bias support
- Vertex Fog and Fog Table
- Specular Lighting
- Alpha Blending
- High quality dithering
- ROP2 support

- Internal full 32-bit ARGB format for high rendering quality

Display Controller Block Diagram



LCD Panel Interface Signals

Signal	Pin	Type	Description
LCD-B0	P3-126	O	LCD Panel Data Bus.
LCD-B1	P2-95	O	
LCD-B2	P2-97	O	
LCD-B3	P2-100	O	
LCD-B4	P2-99	O	
LCD-B5	P2-102	O	
LCD-G0	P2-101	O	
LCD-G1	P2-104	O	
LCD-G2	P2-106	O	
LCD-G3	P2-105	O	
LCD-G4	P2-108	O	
LCD-G5	P2-107	O	
LCD-R0	P3-128	O	
LCD-R1	P2-109	O	
LCD-R2	P2-113	O	
LCD-R3	P2-116	O	
LCD-R4	P2-118	O	
LCD-R5	P2-117	O	
LCD-SCK	P2-112	O	Display Data Clock. Pixel clock for flat panel data.
LCD-FRM	P2-111	O	Frame Sync. Flat Panel equivalent of VSYNC.
LCD-LP	P2-96	O	Line Sync. Flat Panel equivalent of HSYNC.
LCD-DE	P2-114	O	Display Enable signal (DE) for TFT Panels.
LCD-VDDEN	P3-130	O	Power sequencing control for panel driver electronics voltage VDD.

CRT and TV Interface Signals

Signal	Pin	Type	Output Drive	Description
CRT-HSYNC	P3-129	O	1/4 mA	CRT Horizontal Sync
CRT-VSYNC	P3-140	O	1/4 mA	CRT Vertical Sync
CRT-R	P3-132	O	19 mA	CRT analog video outputs from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g., 75 ohm resistor on the board, in parallel with the 75 ohm CRT load)
CRT-G	P3-136	O	19 mA	
CRT-B	P3-133	O	19 mA	

TV-OUT	P3-138	O	35 mA	Composite Video. Includes synchronization, luminance and chrominance components of video. Available when TV encoder is assembled ("V" option)
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Video Input Port interface signals

Signal	Pin	Type	Description
VIP-CLK	P3-88	I	Video Input Port clock input
VIP-D0	P3-80	I	Video Input Port data input
VIP-D1	P3-82	I	Video Input Port data input
VIP-D2	P3-84	I	Video Input Port data input
VIP-D3	P3-90	I	Video Input Port data input
VIP-D4	P3-92	I	Video Input Port data input
VIP-D5	P3-94	I	Video Input Port data input
VIP-D6	P3-96	I	Video Input Port data input
VIP-D7	P3-89	I	Video Input Port data input

3.4. General Purpose Input / Output

The South Bridge of the CM-iVCF - VT8237, provides 10 general purpose I/O pins (GPIO's), as listed in the following table:

Signal	Pin	Type	Description
GPIO0	P1-13	I/O	GPIO 12 of the south bridge
GPIO1	P1-16	I/O	GPIO 13 of the south bridge
GPIO2	P1-15	I/O	GPIO 14 of the south bridge
GPIO3	P1-18	I/O	GPIO 15 of the south bridge
GPIO4	P3-37	I/OD	GPIO 20 of the south bridge
GPIO5	P3-40	I/OD	GPIO 21 of the south bridge
GPIO6	P3-39	I/OD	GPIO 22 of the south bridge
GPIO7	P3-42	I/OD	GPIO 23 of the south bridge
GPIO8	P3-41	I/OD	GPIO 28 of the south bridge
GPIO9	P3-44	I/OD	GPIO 29 of the south bridge

* OD - Open Drain

GPIO's of Super-I/O chip

The Super I/O chip provides thirteen input/output pins routed to interface connectors. These can be individually configured to perform a simple I/O function or a pre-defined alternate function. I/O pins are divided into two groups - Port 1 and Port3, each group containing up to eight pins. (Port 2 pins are not available on connector). Port 1 pins are configured through control registers in logical device 7, Port3 pins in logical device 9. Users can configure each individual pin to be an input or an output port by programming the respective bit in the selection register (CRF0: 0 = output, 1 = input). Invert the port value by setting the inversion register (CRF2: 0 = non-inverse, 1 = inverse). The pin value is read/written through data register (CRF1).

Super I/O GPIO Signals of Port 1

Signal	Pin	Type	Description
GPIO10	P3-46	I/OD12	SIO General purpose I/O port 1 bit 0
GPIO11	P3-45	I/OD12	SIO General purpose I/O port 1 bit 1
GPIO12	P3-48	I/OD12	SIO General purpose I/O port 1 bit 2
GPIO13	P3-47	I/OD12	SIO General purpose I/O port 1 bit 3
GPIO14	P3-49	I/OD12	SIO General purpose I/O port 1 bit 4
GPIO15	P3-52	I/OD12	SIO General purpose I/O port 1 bit 5
GPIO16	P3-54	I/OD12	SIO General purpose I/O port 1 bit 6
GPIO17	P3-56	I/OD12	SIO General purpose I/O port 1 bit 7

- I/OD12 - Input / Open Drain Output. Pulls 12 mA to GND. Requires external pullup resistor.

Super I/O GPIO Signals of Port 3

Signal	Pin	Type	Description
GPIO18	P3-58	I/OD12	General purpose I/O port 3 bit 0
GPIO19	P3-60	I/OD12	General purpose I/O port 3 bit 1
SPARE0	P1-12	I/OD12	General purpose I/O port 3 bit 2
SPARE0	P2-4	I/OD24	General purpose I/O port 3 bit 3
SPARE7	P3-105	I/OD12	General purpose I/O port 3 bit 4

3.5. PCI Bus Host Bridge

The CM-iVCF's South Bridge contains an integrated PCI bus host bridge allowing an interface with any PCI bus Revision 2.2-compliant master or target device. The PCI host bridge on the CM-iVCF has the following functionality:

- **Master controller**—Allows the CPU to be a master on the PCI bus. The CPU can generate transactions to configure the PCI host bridge, as well as all external devices on the PCI bus. The CPU can also generate memory and I/O read and write transactions on the PCI bus.
- **Target controller**—Allows external PCI bus masters to access the CM-iVCF's on-board DRAM.

Features:

- 33 MHz operation
- Supports up to four PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec (north bridge data transfer via high speed V-Link)
- PCI master snoop ahead and snoop filtering
- Eight DW of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

PCI Clock System

The clock source is from an on-board oscillator. The CM-iVCF acts as a 'motherboard', providing clocks to all other parts of the application. If a developer needs to synchronize PCI bus operation with another clock source from a custom baseboard, then a PCI-to-PCI bridge should be used. (Suitable bridges are available from PLX and other manufacturers.)

The PCI standard allows up to a 2ns clock skew. In order to minimize the initial skew value, the internal feedback path is designed with a 10 cm trace length - to create the initial delay. Feedback is provided to the clock generation block of the PCI bridge. The timing of all internal clock references is shifted accordingly. In other words, PCI signals are pre-compensated for an external clock trace length of 10 cm. The maximum allowed length of the external clock trace is:

10 cm (pre-compensated) + 30 cm (max propagation delay for a skew less than 2ns)

PCI Bus Signals

CAMI conn		Type	Description
Signal	Pin		
PCI-AD0	P2-20	B	PCI Address Data Bus is the PCI time-multiplexed PCI_address / PCI_data / sub_ISA bus.
PCI-AD1	P2-22	B	
PCI-AD2	P2-21	B	
PCI-AD3	P2-24	B	
PCI-AD4	P2-23	B	
PCI-AD5	P2-25	B	
PCI-AD6	P2-28	B	
PCI-AD7	P2-27	B	
PCI-AD8	P2-29	B	
PCI-AD9	P2-32	B	
PCI-AD10	P2-34	B	
PCI-AD11	P2-33	B	
PCI-AD12	P2-36	B	
PCI-AD13	P2-35	B	
PCI-AD14	P2-37	B	
PCI-AD15	P2-40	B	
PCI-AD16	P2-51	B	
PCI-AD17	P2-54	B	
PCI-AD18	P2-53	B	
PCI-AD19	P2-56	B	
PCI-AD20	P2-58	B	
PCI-AD21	P2-57	B	
PCI-AD22	P2-60	B	
PCI-AD23	P2-59	B	
PCI-AD24	P2-64	B	
PCI-AD25	P2-63	B	
PCI-AD26	P2-66	B	
PCI-AD27	P2-65	B	
PCI-AD28	P2-68	B	
PCI-AD29	P2-70	B	
PCI-AD30	P2-69	B	
PCI-AD31	P2-72	B	

PCI Bus Signals (continued)

CAMI conn		Type	Description
Signal	Pin		
PCI-CBE0#	P2-30	B	Command or Byte-Enable Bus functions: (1) as a time-multiplexed bus command that defines the type of transaction on the AD bus, or (2) as byte enables: CBE0 for AD7–AD0
PCI-CBE1#	P2-39	B	Command or Byte-Enable Bus functions: (1) as a time-multiplexed bus command that defines the type of transaction on the AD bus, or (2) as byte enables: CBE1 for AD15–AD8
PCI-CBE2#	P2-52	B	Command or Byte-Enable Bus functions: (1) as a time-multiplexed bus command that defines the type of transaction on the AD bus, or (2) as byte enables: CBE2 for AD23–AD16
PCI-CBE3#	P2-61	B	Command or Byte-Enable Bus functions: (1) as a time-multiplexed bus command that defines the type of transaction on the AD bus, or (2) as byte enables: CBE3 for AD31–AD24
PCI-DEVSEL#	P2-45	B	Device Select is asserted by the target when it has decoded its address as the target of the current transaction. This signal is pulled up on-board with an 8.2K resistor.
PCI-FRAME#	P2-49	B	Frame is driven by the transaction initiator to indicate the start and duration of the transaction. This signal is pulled up on-board with an 8.2K resistor.
PCI-INTA#	P2-6	I	PCI Interrupt Requests is asserted to request an interrupt. Configuration registers allow inversion of these interrupt requests to recognize active low interrupt requests.
PCI-INTB#	P2-8	I	
PCI-INTC#	P3-20	I	
PCI-INTD#	P3-17	I	
PCI-IRDY#	P2-47	B	Initiator Ready is asserted by the current bus master to indicate that data is ready on the bus (write) or that the master is ready to accept data (read). This signal is pulled up on-board with an 8.2K resistor.
PCI-PAR	P2-42	B	PCI Parity is driven by the initiator or target to indicate parity on the AD31–AD0 and CBE3–CBE0 busses.
PCI-PERR#	P2-44	B	Parity Error is asserted to indicate a PCI bus data parity error in the previous clock cycle. This signal is pulled up on-board with an 8.2K resistor.

CAMI conn		Type	Description
Signal	Pin		
PCI-PCIRST#	P1-137	O	Reset is asserted to reset the PCI devices.
PCI-SERR#	P2-41	I	System Error is used for reporting address parity errors or any other system error where the result is fatal. This signal is pulled up on-board with an 8.2K resistor.
PCI-STOP#	P2-46	B	Stop is asserted by the target to request that the current bus transaction be stopped. This signal is pulled up on-board with an 8.2K resistor.
PCI-TRDY#	P2-48	B	Target Ready is asserted by the currently addressed target to indicate its ability to complete the current data phase of a transaction. This signal is pulled up on-board with an 8.2K resistor.

PCI-REQ0# PCI-REQ1# PCI-REQ2# PCI-REQ3#	P2-1 P2-18 P3-22 P3-13	I	Bus Request is asserted by the master to request access to the bus.
PCI-GNT0# PCI-GNT1# PCI-GNT2# PCI-GNT3#	P2-3 P2-5 P3-18 P3-15	O	Bus Grant is asserted by the CM-iVCF to grant access to the bus.
PCI-CLK0 PCI-CLK1 PCI-CLK2	P2-16 P3-16 P3-24	O	PCI Bus Clock Output is a 33-MHz clock for PCI bus devices. This signal is derived from an onboard 33MHz source. Clock edge position is internally compensated in order to reduce skew to a minimum.

Notes

1. Output drive and maximum load specifications are according to PCI bus Standard Rev-2.2.
2. PCI Bus inputs / outputs inputs are 3.3V-level, 5V tolerant.

PCI resource map

Device	IDSEL line	PCI dev. / func.	IRQ
ATX baseboard PCI Slot	AD18	0x07, func. 0	10,11
ATX baseboard CardBus bridge skt. A	AD19	0x08, func. 0	11
ATX baseboard CardBus bridge skt. A	AD19	0x08, func. 1	10
ATX BASEBOARD Ethernet	AD20	0x09, func. 0	10
CM-iVCF SATA / RAID controller	AD26	0x0F, func. 0	11
CM-iVCF IDE controller	AD26	0x0F, func. 1	14
USB 1.1 controller	AD27	0x10, func. 0	10
USB1.1 controller	AD27	0x10, func. 1	10
USB 1.1 controller	AD27	0x10, func. 2	11
USB 1.1 controller	AD27	0x10, func. 3	11
USB 2.0 controller	AD27	0x10, func. 4	9
USB device controller	AD27	0x10, func. 5	5
CM-iVCF internal ISA bridge	AD28	0x11, func. 0	-
CM-iVCF audio controller	AD28	0x11, func. 5	9
CM-iVCF Ethernet controller	AD29	0x12, func. 0	10
CM-iVCF display controller	-	0x00, func. 0, bus 1	11

PCI devices have no hardcoded IRQ assignment. The IRQ assignment listed in the table is correct for CM-iVCF plugged into CompuLab's baseboard (such as ATX), but can change if additional hardware attached.

3.6. AC97 Interface

The audio / modem link in the CM-iVCF is AC97 Revision 2.2 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality two-speaker audio solution. Audio codec is included on-board in the CM-iVCF.

Features Supported by AC97:

- AC-Link access to 2 CODECs (AC97 or AMC97 or MC97)
- Multichannel Audio
- Bus Master Scatter / Gather DMA
- Dedicated read and write channels supporting simultaneous stereo playback and record
- Dedicated read and write channels supporting simultaneous modem receive and transmit
- 32-byte line-buffers for each SGD channel
- Programmable 8bit / 16bit mono / stereo PCM data format support
- AC97 2.2 compliant

By using an optional audio codec, the CM-iVCF module implements cost-effective, high quality, integrated audio. In addition, an AC97 soft modem can be implemented with the use of a modem codec.

AC97 link signals

CAMI conn		Type	Description
Signal	Pin		
AC97-RST#	P3-124	O	AC97 Reset: Master H/W reset to external Codec(s)
AC97-SYNC	P3-125	O	AC97 Sync: 48 KHz fixed rate sample sync to the Codec(s)
AC97-BITCLK	P3-120	I	AC97 Bit Clock: 12.288 MHz serial data clock generated by the external Codec(s).
AC97-SDOUT	P3-123	O	AC97 Serial Data Out: Serial TDM data output to the Codec(s). AC_SDOOUT is sampled at the rising edge of PWROK as a functional strap.
AC97-SDIN0	P3-119	I	AC97 Serial Data In 0: Serial TDM data input from a Codec. The on-board Codec uses this line.
AC97-SDIN1	P3-121	I	AC97 Serial Data In 1: Serial TDM data input from a Codec.

3.7. LPC - Low Pin Count Interface

The CM-iVCF implements an LPC Interface and Controller as described in the LPC 1.0 specification. The LPC bus provides a functional replacement for interfacing of legacy ISA functions, such as an additional Super-I/O chip.

LPC bus signals

CAMI conn		Type	Description
Signal	Pin		
LPC-LAD0	P2-10	I/O	LPC Multiplexed Command, Address, Data.
LPC-LAD1	P2-9	I/O	
LPC-LAD2	P2-12	I/O	
LPC-LAD3	P2-11	I/O	
LPC-LDRQ#	P2-17	I	LPC Serial DMA/Master Request Inputs: DMA or bus master request.
LPC-LFRAME#	P2-15	O	LPC Frame: Indicates the start of an LPC cycle, or an abort.

In addition to the above signals, an LPC device needs a PCI clock and the PCIRST# signal.

3.8. Serial Ports

The CM-iVCF includes two optional serial ports (UARTs) available when Super-I/O chip is assembled. The UART's power up as 16450-compatible devices. They are switched to 16550 (FIFO) mode under control of serial drivers, specific to the operating system used. In FIFO mode, the receive and transmit circuitry are each enhanced by separate 16-byte FIFO's to off-load the CPU from repetitive service routines.

The serial ports include the following features:

- Full modem control lines
- Separately enabled receiver line status, receiver data, character timeout, transmitter holding register, and modem status interrupts
- A Baud rate generator providing input a clock divisor from 1 to 65535 to create a 16x clock
- 5-, 6-, 7-, or 8-bit data
- Even, odd, stick, or no parity generation and checking
- 1, 1-1/2 or 2 stop-bit generation
- Break generation/detection

- Baud rate up to 1.5 Mbaud.

First UART includes RS232 drivers, the other UART have a TTL signal level interface.

Serial Port Signals

CAMI conn		Interf	Type	Description
Signal	Pin			
COMA-RX	P1-22	RS232	I	Serial Data In receives the serial data from the external serial device or DCE into the internal serial port controller.
COMB-RX	P1-23	TTL	I	
COMA-TX	P1-24	RS232	O	Serial Data Out transmits the serial data from the internal serial port controller to the external serial device or DCE.
COMB-TX	P1-25	TTL	O	
COMA-CTS	P3-27	RS232	I	Clear To Send is driven back to the serial port to indicate that the external data carrier equipment (DCE) is ready to accept data.
COMB-CTS	P3-33	TTL	I	
COMA-DCD	P3-21	RS232	I	Data Carrier Detect is driven back to the serial port from data carrier equipment when it detects a carrier signal from a communications target.
COMB-DCD	P3-29	TTL	I	
COMA-DSR	P3-25	RS232	I	Data Set Ready indicates that the external DCE is ready to establish a communication link with the serial port controller.
COMB-DSR	P3-35	TTL	I	
COMA-DTR	P3-23	RS232	O	Data Terminal Ready indicates to the external DCE that the serial port controller is ready to communicate.
COMB-DTR	P3-36	TTL	O	
COMA-RIN	P3-30	RS232	I	Ring Indicate is used by an external modem to inform the serial port that a ring signal was detected. A change in state on this signal by the external modem can be configured to cause a modem status interrupt.
COMB-RIN	P3-34	TTL	I	
COMA-RTS	P3-28	RS232	O	Request To Send indicates to the external DCE that the internal serial port controller is ready to send data.
COMB-RTS	P3-32	TTL	O	

3.9. Infrared Port

The CM-iVCF provides an infrared port designed for systems supporting infrared communication compliant with the Infrared Data Association (IrDA) standard.

Infrared Port Signals

CAMI conn		Type	Description
Signal	Pin		
IRDA-RX	P2-123	I	Infrared Serial Input is the digital input for the serial infrared interface.
IRDA-TX	P2-121	O	Infrared Serial Output is the digital output for the serial infrared interface.

3.10. Parallel Port

The CM-iVCF incorporates a PC/AT compatible parallel port, available when a Super-I/O chip is assembled. It supports bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. The Super-I/O configuration registers allow disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The Parallel Port interface includes minimal passive components required for its operation. Serial dumping resistors and the protection circuitry (required in order to prevent possible damage due to printer power-up or ESD) are not included, and should be added externally if required.

Parallel Port Signals

CAMI conn		Type	Description
Signal	Pin		
PP-SLCTIN#	P2-93	O	Printer Select Input. This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register.
PP-INIT#	P2-89	O	Initiate Output. This output is bit 2 of the printer control register. This is used to initiate the printer.
PP-ALF#	P2-85	O	Auto line feed. This output goes low to cause the printer to automatically feed a line after each line that is printed. The AUTOFD output is the complement of bit 1 of the Printer Control Register.

CAMI conn		Type	Description
Signal	Pin		
PP-STROBE#	P2-83	O	Strobe Output. An active low pulse on this output is used to strobe the printer data into the printer. The STROBE output is the complement of bit 0 of the Printer Control Register.
PP-BUSY	P2-90	I	Busy Status Input. This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
PP-ACK#	P2-88	I	Acknowledge. An active low output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACK input.
PP-PE	P2-92	I	Paper End. Status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
PP-SCLT	P2-94	I	Printer Selected Status. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
PP-ERROR#	P2-87	I	Printer Error. A low on this input from the printer indicates that there is an error condition at the printer. Bit 3 of the Printer Status register reads the ERR input.
PP-PD0	P2-81	I/O	Port Data. The bi-directional parallel data bus is used to transfer information between the parallel port and peripherals.
PP-PD1	P2-77		
PP-PD2	P2-75		
PP-PD3	P2-76		
PP-PD4	P2-78		
PP-PD5	P2-80		
PP-PD6	P2-82		
PP-PD7	P2-84		

3.11. PS/2 Keyboard and Mouse Interface

The PS/2 interface circuit is found in the VT8237 South Bridge. It is designed to provide the functions needed to interface a CPU with legacy keyboard and mouse. Note that in modern application PS/2 keyboard and mouse interface is substituted by USB interface, which is also provided by CM-iVCF.

PS/2 Interface Signals

CAMI conn		Type	Description
Signal	Pin		
PS2-KDAT	P2-119	I/O	Keyboard Data
PS2-KCLK	P2-120	I/O	Keyboard Clock
PS2-MDAT	P2-124	I/O	Mouse Data
PS2-MCLK	P2-126	I/O	Mouse Clock

3.12. USB Ports

The CM-iVCF provides four complete, independent USB 2 ports. The USB ports are Host Controller Interface (HCI) compliant. The HCI specification provides a register level description for a host controller, as well as common industry hardware/software interface and drivers. USB ports are supported by all O/S packages provided for CM-iVCF.

Features:

- USB v2.0 / EHCI v1.0 and USB v1.1 / UHCI v1.1 compatible
- Physical layer transceivers with optional over-current detection status on USB inputs
- Eighteen level (doublewords) data FIFO with full scatter and gather capability

USB Port Signals

CAMI conn		Type	Description
Signal	Pin		
USB-OVC#	P2-133	I	Overcurrent. This signal indicates that the USB hub has detected an overcurrent on the USB. This pin has a 8.2k pull-up
USB1-N	P2-140	I/O	USB Port 1 Data Negative for Port 1
USB1-P	P2-138	I/O	USB Port 1 Data Positive for Port 1
USB2-N	P2-139	I/O	USB Port 2 Data Negative for Port 2
USB2-P	P2-137	I/O	USB Port 2 Data Positive for Port 2
USB3-N	P1-138	I/O	USB Port 3 Data Negative for Port 3
USB3-P	P1-136	I/O	USB Port 3 Data Positive for Port 3
USB4-N	P1-139	I/O	USB Port 4 Data Negative for Port 4
USB4-P	P1-137	I/O	USB Port 4 Data Positive for Port 4

3.13. Audio Interface

The CM-iVCF implements audio interface using Phillips UCB1400 codec chip which also includes touch screen controller. The codec is an AC'97 2.1 compliant stereo audio codec designed for PC multimedia systems. It uses industry-leading delta-sigma and mixed signal technology. This advanced technology and its features are designed to help in enabling the design of PC 99 and PC 2001 compliant high-quality audio systems. The codec surpasses PC 99, PC 2001 and AC '97 2.1 audio quality standards. The audio system also includes a power amplifier for matching the stereo output for a direct connection of stereo headphones.

Features

- Integrated High-Performance Headphone Amplifier
- Sample Rate Converters
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Line-level Stereo Input for LINE IN
- Microphone Input
- Integrated High-Performance Microphone Pre-Amplifier
- Meets or Exceeds the Microsoft PC 99 and PC 2001 Audio Performance Requirements

Audio specifications

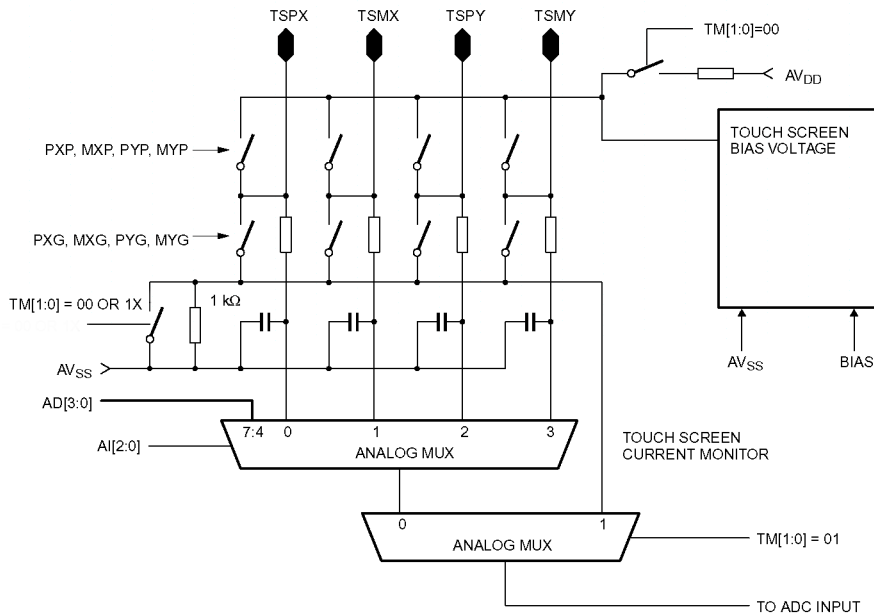
Speaker Output	Type	Stereo
	Power	25 mW/ch into 32 ohm speakers
	Decoupling	Requires external 220uF capacitors, for 8 ohm load. Smaller capacitors (like 1uF) can be used for high-impedance loads.
Microphone Input	Type	Mono, electret or dynamic
	Decoupling	On-board
Line Input	Type	Stereo
	Decoupling	On-board

Audio Interface Signals

Signal	Pin Number	Type	Output Drive	Description
AUD-INL-MIC	P2-132	I	-	Audio stereo line input left and microphone mono input.
AUD-INR	P2-130	I	-	Audio stereo line input right.
AUD-OUTL	P2-131	O	25 mW	Speaker stereo output left. Can be used as line output.
AUD-OUTR	P2-136	O	25 mW	Speaker stereo outputs right. Can be used as line output.

3.14. Touch Screen Controller

The optional UCB1400 codec chip includes universal touch screen controller. Touch screen interface is for 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. Touch screen interface is fully supported by drivers in O/S packages provided by CompuLab.



The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or

grounded in the touch screen switch matrix. Each of the four touch screen signals can be selected as input for the built-in 10-bit ADC, which is used to determine the voltage on the selected touch screen pin in position measurement mode. In addition, the UCB1400 can monitor touch screen current via an internal 1 Kohm resistor that can act as the input to the 10-bit ADC in pressure or plate resistance measurement mode. The flexible switch matrix and the multi-functional touch screen bias circuit enable the user of the UCB1400 to set each desired touch screen configuration.

The UCB1400's internal voltage reference (V_{ref}) acts as the reference voltage for the touch screen bias circuitry. This makes the touch screen biasing independent of supply voltage and temperature variations. Four low pass filters, one on each touch screen terminal, are built in to minimize the noise coupled from the LCD into the touch screen signals. An LCD typically generates large noise glitches on the touch screen, since they are closely coupled.

Touch Screen Interface Signals

Signal	Pin Number	Type	Description
TS-PX	P1-53	Analog	Plate X, plus (Left)
TS-MX	P2-71	Analog	Plate X, minus (Right)
TS-PY	P1-57	Analog	Plate Y, plus (Top)
TS-MY	P2-73	Analog	Plate Y, minus (Bottom)

"A" - Analog type

3.15. Harddisk Controller 1 - Parallel ATA

- Single channel hard disk controller supporting two Enhanced IDE devices
- Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface
- Increased reliability using UltraDMA-133/100/66/33 transfer protocols
- Thirty-two levels (doublewords) of prefetch and write buffers
- DMA engine for concurrent operation
- Bus master programming interface for SFF-8038i rev.1.0 and Windows compliant
- Full scatter gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support under Linux and Windows

Harddisk Controller 1 (Parallel ATA) interface is shared with local bus. These two functions are mutually exclusive. Developer can utilize Serial ATA interface if both local bus and external harddisk are required in the system.

Harddisk Interface Signals

Note: connector signal names reflect naming of PIO mode. In DMA modes signal functionality redefined.

CAMI conn		Type	Description
Signal	Pin		
IDE-CS0#	P1-47	O	IDE Device Chip Select for 1F0h Range: for ATA command register block.
IDE-CS1#	P1-52	O	IDE Device Chip Select for 3F6h Range: for ATA control register block.
LB-A0	P1-64	O	IDE Device Address: Used to indicate which byte in either the ATA command block or control block is being addressed.
LB-A1	P1-63	O	
LB-A2	P1-66	O	
LB-D0	P1-94	I/O	IDE Device Data. IDE Address and Data lines are shared with "Local Bus" pins on CAMI connectors.
LB-D1	P1-95	I/O	
LB-D2	P1-96	I/O	
LB-D3	P1-97	I/O	
LB-D4	P1-100	I/O	
LB-D5	P1-99	I/O	
LB-D6	P1-102	I/O	
LB-D7	P1-101	I/O	
LB-D8	P1-104	I/O	
LB-D9	P1-105	I/O	
LB-D10	P1-106	I/O	
LB-D11	P1-107	I/O	
LB-D12	P1-108	I/O	
LB-D13	P1-109	I/O	
LB-D14	P1-112	I/O	
LB-D15	P1-111	I/O	
IDE-DREQ	P3-63	I	IDE Device DMA Request: asserted by the IDE device to request a data transfer.
IDE-DACK#	P3-65	O	IDE Device DMA Acknowledge: asserted to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of RD# or WR#) is a DMA data transfer cycle.

CAMI conn		Type	Description
Signal	Pin		
IDE-RD#	P1-46	O	<p>Disk I/O Read (PIO mode): the command to the IDE device that it may drive data onto the IDE-D lines. Data is latched on the de-assertion edge of IDE-RD#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0#, IDE-CS1#) and the IDE-A lines, or the IDE DMA acknowledge (IDE-DACK#).</p> <p>Disk Write Strobe (UDMA Writes to Disk): This is the data write strobe for writes to disk.</p> <p>Disk DMA Ready (UDMA Reads from Disk): This is the DMA ready for reads from disk.</p>
IDE-WR#	P1-48	O	<p>Disk I/O Write (PIO and Non-UDMA): the command to the IDE device that it may latch data from the IDE-D lines. Data is latched by the IDE device on the de-assertion edge of IDE-WR#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0, IDE-CS1) and the IDE-A line, or the IDE DMA acknowledge (IDE-DACK#).</p> <p>Disk Stop (UDMA): the controller asserts this signal to terminate a burst.</p>
LB-IORDY	P1-113 P3-66	I	<p>I/O Channel Ready (PIO): keeps the strobe active (IDE-RD# or IDE-WR#) longer than the minimum width. It adds wait states to PIO transfers.</p> <p>Disk Read Strobe (UDMA Reads from Disk): When reading from the disk, the controller latches data on rising and falling edges of this signal from the disk.</p> <p>Disk DMA Ready (UDMA Writes to Disk): When writing to the disk, this is de-asserted by the disk to pause burst data transfers. This signal has an internal 1.5k pull-up.</p>

3.16. Harddisk Controller 2 - Serial ATA

- One Serial ATA channel, complies with specification Rev 1.0
- On-chip Serial ATA (S-ATA) PHY for supporting of S-ATA device directly
- S-ATA drive transfer rate is capable of up to 150 MB/s per (serial speed of 1.5 Gbit/s)

Signal	Pin	Type	Description
FW-TPBM	P3-51	A/O	SATA-TXP Serial ATA positive transmit signal
FW-TPBP	P3-53	A/O	SATA-TXM Serial ATA negative transmit signal

FW-TPAP	P3-57	A/I	SATA-RXP Serial ATA positive receive signal
FW-TPAM	P3-59	A/I	SATA-RXM Serial ATA negative receive signal

Serial ATA interface uses pins originally reserved in CAMI connector for FireWire function, which is not implemented in CM-iVCF.

3.17. Floppy Disk Controller

The Floppy Disk Controller (FDC) provides the interface to floppy disk drives. The FDC is available only if an optional Super-I/O chip is assembled. Floppy disk signals shared with LPT port and are available through LPT port interface.

Floppy Disk Interface through LPT

LPT Connector (DB26) Pin	SPP Mode	Pin Direction	FDC Mode	Pin Direction
1	STB	I/O	(DS0)	I/(0)
2	PD0	I/O	INDEX	I
3	PD1	I/O	TRKO	I
4	PD2	I/O	WP	I
5	PD3	I/O	RDATA	I
6	PD4	I/O	DSKCHG	I
7	PD5	I/O	MEDIA-ID0	I
8	PD6	I/O	(MTR0)	I/(0)
9	PD7	I/O	MEDIA-ID1	I
10	ACK	I	DS1	0
11	BUSY	I	MTR1	0
12	PE	I	WDATA	0
13	SLCT	I	WGATE	0
14	AFD	I/O	DENSEL	0
15	ERR	I	HDSEL	0
16	INIT	I/O	DIR	0
17	SLIN	I/O	STEP	0

3.18. 10/100 Mbit Ethernet Port

The CM-iVCF contains one full-featured 10/100 Mbit Ethernet interface. The Ethernet interface is based on MAC function provided by VT8237 South Bridge and additional on-board PHY.

- High performance PCI master interface with scatter / gather and bursting capability
- On-board PHY
- 10 / 100 Mbps full and half duplex operation
- Independent 2K byte FIFOs for receive and transmit
- Physical, Broadcast, and Multicast address filtering using hashing function
- Software controllable power down

Magnetic Modules

The CM-iVCF's Twisted Pair interface requires an external transformer (magnetic module) for interface to an RJ-45 connector. Two options exist:

1. An RJ-45 connector with a built-in transformer. Examples:

Vendor	Model
YCL	PTC1111-01
PCA	EPJ9025
Bothhand	LUIS041C

2. A separate transformer and RJ-45 connector. Examples of available transformers:

Vendor	Model
Delta	LF8200A
Pulse Engineering	PE-68515
Pulse Engineering	H1012

Routing Ethernet Signals

The following rules should be applied when routing differential transmit and receive signals between the CM-iVCF interface connector and an external connector/transformer module:

1. Route the differential signal pairs (TXN, TXP) and (RXN, RXP) in parallel, with minimal and consistent clearance within the pair. The distance between RX and TX pairs should be maximized, otherwise TX will induce crosstalk into RX.

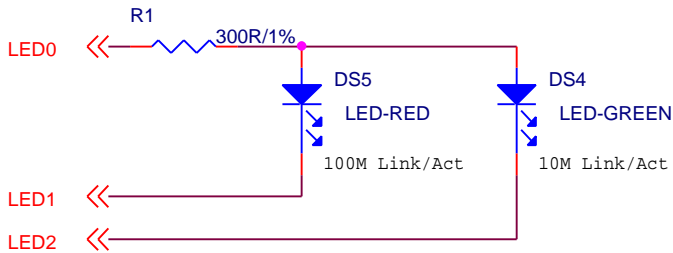
2. It is preferable (but not mandatory) to keep the trace length of Ethernet signals as short as possible. If trace length exceeds 2 inches, additional steps, not specified here, should be taken. Recommended trace width: 5 to 8 mil.
3. Don't route any other traces nearby or across the Ethernet signals' path.
4. It is preferable (but not mandatory) to remove the ground and other planes from beneath the Ethernet trace area.

The listed rules cover the routing requirements if an RJ-45 connector with a built-in transformer is used. If a separate transformer is used, additional rules should be followed for transformer-to-connector routing.

Ethernet Port Signals

CAMI conn		Type	Output Drive	Description
Signal	Pin			
ETH1-TDN ETH1-TDP	P1-3 P1-1	A/O		Analog Twisted Pair Ethernet Transmit Differential Pair. These signals interface directly with an isolation transformer. TDP and TDN pins are connected by a 100 ohm termination resistor.
ETH1-RDN ETH1-RDP	P1-2 P1-4	A/I		Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. RDP and RDN pins are connected by a 100 ohm termination resistor.
ETH1- ACT# (LED0)	P1-10	O	10 mA	Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH1- LINK100# (LED1)	P1-5	O	10 mA	100 Link LED. The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH1- LINK10# (LED2)	P1-6	O	10 mA	10 Link LED. The 10 Link LED pin indicates link integrity and 10 or 100 Mbps connection speed.

Recommended LED connection



This connection supplies full information about speed/link/activity.

LED-RED with LED-GREEN : 100 Mbps link / activity indicator
 LED-GREEN : 10 Mbps link / activity indicator

Activity	LED (Red/Green)
none	off
Link (only)	on
Tx / Rx (and Link)	blink

3.19. Analog inputs

The on-board SIO has five Analog to Digital converters of 8-bit.

CAMI conn		SIO Name	Description
Signal	Pin		
SPARE	P3-9	VCOREB	0V to 4.096V FSR Analog Input.
SPARE	P3-11	+3.3VIN	-//-
SPARE	P3-12	+12VIN	-//-
SPARE	P3-97	-12VIN	-//-
SPARE	P3-101	-5VIN	-//-

Notes

1. The "SIO Name" column exists to help in finding the specific channel information in the SIO datasheet.
2. In no event shall the voltage applied to these inputs surpass the range of 0 to 4.096V.

3.20. Local Bus

CM-iVCF implements local bus functionality using IDE channel. (Note that in CAMI connectors specifications, local bus and IDE interface are sharing the same pins). Driver provided in O/S packages enables access to simple devices connected directly to data, address and control lines of IDE interface. The following IDE signals are in use:

Signal	Pin	Type	Description
LB-A0	P1-64	O	Device Address: Used to indicate byte address within address range of active Chip Select. Note: 8-bit unaligned access is not supported.
LB-A1	P1-63	O	
LB-A2	P1-66	O	
LB-D0	P1-94	I/O	Device Data.
LB-D1	P1-95	I/O	
LB-D2	P1-96	I/O	
LB-D3	P1-97	I/O	
LB-D4	P1-100	I/O	
LB-D5	P1-99	I/O	
LB-D6	P1-102	I/O	
LB-D7	P1-101	I/O	
LB-D8	P1-104	I/O	
LB-D9	P1-105	I/O	
LB-D10	P1-106	I/O	
LB-D11	P1-107	I/O	
LB-D12	P1-108	I/O	
LB-D13	P1-109	I/O	
LB-D14	P1-112	I/O	
LB-D15	P1-111	I/O	
IDE-RD#	P1-46	O	Data Read Strobe: the command to the device that it may drive data onto the D0:D15 lines. Data is latched on the de-assertion edge of RD#. Active only in local bus address window A00h to A07h.
IDE-WR#	P1-48	O	Data Write Strobe: the command to the device that it may latch data from the D0:D15 lines. Data is latched by the device on the de-assertion edge of WR#. Active only in local bus address window A00h to A07h.
LB-IORDY	P1-113 P3-66	I	I/O Channel Ready: keeps the strobe active (RD# or WR#) longer than the minimum width. It adds wait states to PIO transfers. This signal has an internal 1.5k pull-up.

IDE-IRQ	P1-49	I	Normally assigned as IRQ14, this interrupt input can be used for general purpose devices. User's device driver is responsible to handle the interrupt in case that interrupt is used.
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Local Bus interface doesn't have dedicated Chip Select signal specifying address window. Instead, provided RD# and WR# signals are specific for local bus address range - A00h to A07h. RD# and WR# signals are activated only in that window.

Local Bus Timing

Local bus signals are synchronized with PCI clock. The programmable signals can be changed in PCI clock (30 ns) increments.

Tact	150 ns 30-500 ns	Read / Write active pulse width, default Programmable range
Tinact	500 ns	Inactive time between two adjacent cycles

Local bus is shared with primary Harddisk controller (Parallel ATA #0) interface. These two functions are mutually exclusive. Developer can utilize Serial ATA interface if both local bus and external harddisk are required in the system.

3.21. Clocks, Timers, Reset, Write Protect, Boot, PWM

CAMI conn		Type	Comment
Signal	Pin		
RST-IN#	P1-11	I	Reset input, active low. Low level on this pin initiates hardware reset of CM-iVCF. The CM-iVCF will exist reset state 1 second after deactivation of RESET-IN. This pin is not mandatory for CM-iVCF operation, as it generates power-on reset using on-board circuitry. It has internal pullup and can be left unconnected.
RST-OUT#	P1-137	ODP	Reset output, active low. Indicates that CM-iVCF undergoes hardware reset, due to powerup or RESET-IN. Can be used as reset signal to off-board hardware. RESET-OUT minimum duration is approximately 0.5 seconds. The output type is open drain with 10K pullup resistor.
WP1#	P1-9	I	BIOS flash write protect. Writes to flash will be disabled if pulled to "0". To enable writes pull this input to 1 or leave unconnected. This input has internal pullup.
WP2#	P3-100	I	NAND flash write protect, active low. NAND flash writes will be disabled if pulled to logical 0. To enable NAND flash writes pull this input to 1 or leave unconnected. This input has internal pullup.
SPARE	P3-108	O	PWM0 output of Super I/O
SPARE	P1-112	O	PWM0 output of Super I/O
CLKOUT	P3-76	O	14.318 MHz clock output
TIMER-OUT	P3-61	O	General purpose timer of VT8237. Normally used as PC speaker in PC-compatible systems.
DEBUG1	P1-56	O	Used for first-time factory programming. Should be left unconnected. Irrelevant for any other purpose.
DEBUG0	P1-58	I	

3.22. SMBus (I2C)

CM-iVCF provides host system management bus interface. This interface is compatible with I2C devices

Signal	Pin	Type	Description
SSI-DOUT SSI-DIN	P1-60 P1-59	I/O	SMBus data
SSI- CLK	P1-61	I/O	SMBus clock

3.23. Power Supply Pins

The CM-iVCF requires 5V and 3.3V for operation. Other supply voltages required for CPU and DDR are generated on-board using switched DC-DC converters.

Power Net Description

Signal	Description
GND	Common ground
VCC3_3	Common 3.3 Volt power supply, 0.5A max, used mainly for peripheral devices.
VCORE	Main power supply, 5V @2.5A (max). CPU, chipset and DDR supplies are derived from VCC5
VCC5	5V main power inputs, additional to VCORE
VCC-RTC	The 3.3 Volt supply pin provides power to the internal real-time clock and on-board static / configuration RAM. This pin can be driven independently of all other power pins. This pin enables the connection of an external lithium battery. The battery is not mandatory for the CM-iVCF, if the RTC function is not required. In this case, the VCC-RTC pin should be left unconnected.

Power Supply Pins

GND	P1-8, P1-14, P1-26, P1-38, P1-50, P1-62, P1-74, P1-86, P1-98, P1-110, P1-122, P1-134, P2-2, P2-14, P2-26, P2-38, P2-50, P2-62, P2-74, P2-86, P2-98, P2-110, P2-122, P2-134 P3-8, P3-14, P3-26, P3- 38, P3-50, P3-62, P3-74, P3-86, P3-98, P3-110, P3-122, P3-134
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VCC3	P1-31, P1-67, P1-103, P1-139 P2-7, P2-43, P2-79, P2-135 P3-19, P3-55, P3-91, P3-127, P3-135
VCORE	P1-7, P1-19, P1-43, P1-55, P1-79, P1-91, P1-115, P1-127 P2-19, P2-31, P2-55, P2-67, P2-91, P2-103, P2-115, P2-127 P3-7, P3-31, P3- 43, P3-67, P3-79, P3-103, P3-115
VCC5	P1-140, P3-131
VCC-RTC	P1-20

3.24. Unsupported Pins

The pins specified in the table below exist on the interface connector; however, they are not supported by CompuLab. Users should not use these pins. They are documented only for consistency with connectors' pinout specifications.

Signal	Pin	Type	Comment
PME	P1-17	I	Power management event / generic SMI source. No software support in CM-iVCF.
SUSP-IN	P1-21	I	Generic SMI source. No software support in CM-iVCF.

3.25. Restrictions On Using Pullups / Pulldowns

Some of the interface pins are also used as CPU pinstrap options. These pinstrap options are not relevant to user, however overriding them will lead to module malfunction. In any design these pins must not have pull-up or pull-down resistors connected and must not be driven by any external source during boot.

Name	Pin	Pinstrap function
AC97-SYNC	P3-125	LPC/FWH BootROM
AC97-SDOUT	P3-123	Watchdog reboot enable
IDE-DACK#	P3-65	External SATA PHY usage
IDE-CS0#	P1-47	Undocumented strap option
IDE-CS1#	P1-52	Undocumented strap option
LB-A0	P1-64	Undocumented strap option
LB-A1	P1-63	Undocumented strap option
LB-A2	P1-66	Undocumented strap option

4. Multiplexed Signal Trade-Offs

Some of VT8237 signals are traded with others to share the same output pins.

Signal Name		Default configuration		Alternate configuration	
CAMI	VT8237				
GPIO4	GPIO20	GPIO	RxE4[6]=1, RxE5[1]=0, PMIO 4C[20]=1	AC97- SDIN2	RxE4[6]=0, RxE5[1]=0, PMIO Rx4C[20]=1
GPIO5	GPIO21	GPIO	RxE4[6]=1, RxE5[2]=0, PMIO 4C[21]=1	AC97- SDIN3	RxE4[6]=0, RxE5[2]=0, PMIO Rx4C[21]=1

Note: alternate functions - SDIN3/4 can be useful for implementations involving multiple (6 or 8) audio channels.

5. Interface Connectors

The CM-iVCF connects to the external world through P1, P2 and P3 - 140-pin, 0.6 mm connectors.

5.1. Connector Type

	Mfg.	CM-iVCF Connector P/N	Mating Connector P/N
P1, P2, P3	AMP	1-5353183-0	1-5353190-0

Standoffs

CM-iVCF has four mounting holes for standoffs. Three of mounting holes - two on bottom side and top left are connected to GND. The bottom left hole is isolated. Refer to mechanical drawing of module with CAMI connectors on page 54. The developer is recommended to connect mating holes of baseboard to GND, in order to improve EMC. The bottom left hole on the baseboard should be isolated, for compatibility with future CAMI modules.

Standoff implemented by three parts: screw, spacer and nut.

	Description	Manufacturer and P/N
Screw	M2, 10 mm length	FCI 95121-005 Acton InoxPro BF22102010 World Bridge Machinery 380J52080
Spacer	M2x.4 thread, 4.2 mm length	Hirosugi ASU-2004 MAC8 2SP-4 World Bridge Machinery M2,L=4mm
Nut	M2, 1.6-2.0mm width	FCI 92869-001 (or 002) Acton InoxPro BG12102000 Bossard 1241397 (DIN934-A2 M2) World Bridge Machinery 381A52000

Mating connectors and standoffs are available from manufacturer representatives or from CompuLab, see [prices] >> [accessories] in CompuLab's website.

5.2. Connector Layout

Bottom side image, viewed from the top side of the module

Board-to-board mating height is 4 mm

Blue colored areas indicate height constrains - don't locate components beneath.

Connector's and mechanical layout is available in DXF format from CompuLab's website, following [\[Developer\]](#) >> [\[CM-iVCF\]](#) >> [\[CM-iVCF - Dimensions and Connectors Location\]](#) links.

5.3. Connectors Pinout

Note: gray-colored signals are not available. They are either not implemented or routed through other pins of the connector (i.e. mixed with other function). Grayed signals are displayed for purpose clarification CAMI standard pin assignment.

	P1-A
P1-02	ETH1-RDN
P1-04	ETH1-RDP
P1-06	ETH1-LINK10#
P1-08	GND
P1-10	ETH1-ACT#
P1-12	SPARE
P1-14	GND
P1-16	GPIO1
P1-18	GPIO3
P1-20	VCC-RTC
P1-22	COMA-RX
P1-24	COMA-TX
P1-26	GND
P1-28	COMC-RX
P1-30	COMC-TX
P1-32	COMC-DCD#
P1-34	COMC-DTR#
P1-36	COMC-DSR#
P1-38	GND
P1-40	COMC-CTS#
P1-42	COMC-RTS#
P1-44	COMC-RIN#
P1-46	IDE-RD#
P1-48	IDE-WR#
P1-50	GND
P1-52	LB/IDE-CS1#
P1-54	LB-IRQ1
P1-56	DEBUG1
P1-58	DEBUG0
P1-60	SSI-DOUT
P1-62	GND
P1-64	LB-A0

	P1-B
P1-01	ETH1-TDP
P1-03	ETH1-TDN
P1-05	ETH1-LINK100#
P1-07	VCORE
P1-09	WP1#
P1-11	RST-IN#
P1-13	GPIO0
P1-15	GPIO2
P1-17	PME#
P1-19	VCORE
P1-21	SUSP-IN
P1-23	COMB-RX
P1-25	COMB-TX
P1-27	COMD-RX
P1-29	COMD-TX
P1-31	VCC3-3
P1-33	COMD-DCD#
P1-35	COMD-DTR#
P1-37	COMD-DSR#
P1-39	COMD-CTS#
P1-41	COMD-RTS#
P1-43	VCORE
P1-45	COMD-RIN#
P1-47	LB/IDE-CS0#
P1-49	IDE-IRQ
P1-51	LB-IRQ0
P1-53	TS-PX
P1-55	VCORE
P1-57	TS-PY
P1-59	SSI-DIN
P1-61	SSI-CLK
P1-63	LB-A1

P1-66	LB-A2
P1-68	LB-A4
P1-70	LB-A6
P1-72	LB-A8
P1-74	GND
P1-76	LB-A10
P1-78	LB-A12
P1-80	LB-A14
P1-82	LB-A16
P1-84	LB-A18
P1-86	GND
P1-88	LB-A20
P1-90	LB-A22
P1-92	LB-A24
P1-94	LB-D0
P1-96	LB-D2
P1-98	GND
P1-100	LB-D4
P1-102	LB-D6
P1-104	LB-D8
P1-106	LB-D10
P1-108	LB-D12
P1-110	GND
P1-112	LB-D14
P1-114	LB-IOCS16#
P1-116	LB-RD# (a)
P1-118	LB-WR# (b)
P1-120	PCM-MEMW# (d)
P1-122	GND
P1-124	PCM-CE1#
P1-126	PCM-CDA#
P1-128	PCM-INT0
P1-130	PCM-WE#
P1-132	PCM-SKTSEL
P1-134	GND
P1-136	USB3-P
P1-138	USB3-N
P1-140	VCC5

P1-65	LB-A3
P1-67	VCC3-3
P1-69	LB-A5
P1-71	LB-A7
P1-73	LB-A9
P1-75	LB-A11
P1-77	LB-A13
P1-79	VCORE
P1-81	LB-A15
P1-83	LB-A17
P1-85	LB-A19
P1-87	LB-A21
P1-89	LB-A23
P1-91	VCORE
P1-93	LB-A25
P1-95	LB-D1
P1-97	LB-D3
P1-99	LB-D5
P1-101	LB-D7
P1-103	VCC3-3
P1-105	LB-D9
P1-107	LB-D11
P1-109	LB-D13
P1-111	LB-D15
P1-113	LB-IORDY
P1-115	VCORE
P1-117	PCM-MEMR# (c)
P1-119	PCM-IOR# (e)
P1-121	PCM-IOW# (f)
P1-123	PCM-WAIT#
P1-125	PCM-RST#
P1-127	VCORE
P1-129	PCM-REG#
P1-131	PCM-CE2#
P1-133	LB-CS0#
P1-135	LB-CS1#
P1-137	RST-OUT#
P1-139	VCC3-3

	P2-A
P2-02	GND
P2-04	SPARE
P2-06	PCI-INTA#
P2-08	PCI-INTB#
P2-10	LPC-LAD0
P2-12	LPC-LAD2
P2-14	GND
P2-16	PCI-CLK0
P2-18	PCI-REQ1#
P2-20	PCI-AD0
P2-22	PCI-AD1
P2-24	PCI-AD3
P2-26	GND
P2-28	PCI-AD6
P2-30	PCI-CBE0#
P2-32	PCI-AD9
P2-34	PCI-AD10
P2-36	PCI-AD12
P2-38	GND
P2-40	PCI-AD15
P2-42	PCI-PAR
P2-44	PCI-PERR#
P2-46	PCI-STOP#
P2-48	PCI-TRDY#
P2-50	GND
P2-52	PCI-CBE2#
P2-54	PCI-AD17
P2-56	PCI-AD19
P2-58	PCI-AD20
P2-60	PCI-AD22
P2-62	GND
P2-64	PCI-AD24
P2-66	PCI-AD26
P2-68	PCI-AD28

	P2-B
P2-01	PCI-REQ0#
P2-03	PCI-GNT0#
P2-05	PCI-GNT1#
P2-07	VCC3-3
P2-09	LPC-LAD1
P2-11	LPC-LAD3
P2-13	LPC-SERIRQ
P2-15	LPC-LFRAME#
P2-17	LPC-LDRQ#
P2-19	VCORE
P2-21	PCI-AD2
P2-23	PCI-AD4
P2-25	PCI-AD5
P2-27	PCI-AD7
P2-29	PCI-AD8
P2-31	VCORE
P2-33	PCI-AD11
P2-35	PCI-AD13
P2-37	PCI-AD14
P2-39	PCI-CBE1#
P2-41	PCI-SERR#
P2-43	VCC3-3
P2-45	PCI-DEVSEL#
P2-47	PCI-IRDY#
P2-49	PCI-FRAME#
P2-51	PCI-AD16
P2-53	PCI-AD18
P2-55	VCORE
P2-57	PCI-AD21
P2-59	PCI-AD23
P2-61	PCI-CBE3#
P2-63	PCI-AD25
P2-65	PCI-AD27
P2-67	VCORE

P2-70	PCI-AD29
P2-72	PCI-AD31
P2-74	GND
P2-76	PP-PD3
P2-78	PP-PD4
P2-80	PP-PD5
P2-82	PP-PD6
P2-84	PP-PD7
P2-86	GND
P2-88	PP-ACK#
P2-90	PP-BUSY
P2-92	PP-PE
P2-94	PP-SLCT
P2-96	LCD-LP
P2-98	GND
P2-100	LCD-B3
P2-102	LCD-B5
P2-104	LCD-G1
P2-106	LCD-G2
P2-108	LCD-G4
P2-110	GND
P2-112	LCD-SCK
P2-114	LCD-DE-M
P2-116	LCD-R3
P2-118	LCD-R4
P2-120	PS2-KCLK
P2-122	GND
P2-124	PS2-MDAT
P2-126	PS2-MCLK
P2-128	PCM-INT-RDYB
P2-130	AUD-INR
P2-132	AUD-INL-MIC
P2-134	GND
P2-136	AUD-OUTR
P2-138	USB1-P
P2-140	USB1-N

P2-69	PCI-AD30
P2-71	TS-MX
P2-73	TS-MY
P2-75	PP-PD2
P2-77	PP-PD1
P2-79	VCC3-3
P2-81	PP-PD0
P2-83	PP-STROBE#
P2-85	PP-ALF#
P2-87	PP-ERROR#
P2-89	PP-INIT#
P2-91	VCORE
P2-93	PP-SLCTIN#
P2-95	LCD-B1
P2-97	LCD-B2
P2-99	LCD-B4
P2-101	LCD-G0
P2-103	VCORE
P2-105	LCD-G3
P2-107	LCD-G5
P2-109	LCD-R1
P2-111	LCD-FRM
P2-113	LCD-R2
P2-115	VCORE
P2-117	LCD-R5
P2-119	PS2-KDAT
P2-121	IRDA-TX
P2-123	IRDA-RX
P2-125	PCM-CDB#
P2-127	VCORE
P2-129	AUD-SPDIF
P2-131	AUD-OUTL
P2-133	USB-OVC#
P2-135	VCC3-3
P2-137	USB2-P
P2-139	USB2-N

	P3-A
P3-02	ETH2-RDP
P3-04	ETH2-RDN
P3-06	ETH2-LINK10#
P3-08	GND
P3-10	ETH2-ACT#
P3-12	SPARE
P3-14	GND
P3-16	PCI-CLK1
P3-18	PCI-GNT2#
P3-20	PCI-INTC#
P3-22	PCI-REQ2#
P3-24	PCI-CLK2
P3-26	GND
P3-28	COMA-RTS#
P3-30	COMA-RIN#
P3-32	COMB-RTS#
P3-34	COMB-RIN#
P3-36	COMB-DTR#
P3-38	GND
P3-40	GPIO5
P3-42	GPIO7
P3-44	GPIO9
P3-46	GPIO10
P3-48	GPIO12
P3-50	GND
P3-52	GPIO15
P3-54	GPIO16
P3-56	GPIO17
P3-58	GPIO18
P3-60	GPIO19
P3-62	GND
P3-64	TIMER-START
P3-66	IDE-RDY#
P3-68	LB-CS2#

	P3-B
P3-01	ETH2-TDN
P3-03	ETH2-TDP
P3-05	ETH2-LINK100#
P3-07	VCORE
P3-09	SPARE
P3-11	SPARE
P3-13	PCI-REQ3#
P3-15	PCI-GNT3#
P3-17	PCI-INTD#
P3-19	VCC3-3
P3-21	COMA-DCD#
P3-23	COMA-DTR#
P3-25	COMA-DSR#
P3-27	COMA-CTS#
P3-29	COMB-DCD#
P3-31	VCORE
P3-33	COMB-CTS#
P3-35	COMB-DSR#
P3-37	GPIO4
P3-39	GPIO6
P3-41	GPIO8
P3-43	VCORE
P3-45	GPIO11
P3-47	GPIO13
P3-49	GPIO14
P3-51	FW-TPBM
P3-53	FW-TPBP
P3-55	VCC3-3
P3-57	FW-TPAP
P3-59	FW-TPAM
P3-61	TIMER-OUT
P3-63	IDE-DREQ
P3-65	IDE-DACK#
P3-67	VCORE

P3-70	LB-CS3#
P3-72	CLKIN
P3-74	GND
P3-76	CLKOUT
P3-78	VIP-CS
P3-80	VIP-D0
P3-82	VIP-D1
P3-84	VIP-D2
P3-86	GND
P3-88	VIP-CLK
P3-90	VIP-D3
P3-92	VIP-D4
P3-94	VIP-D5
P3-96	VIP-D6
P3-98	GND
P3-100	WP2#
P3-102	VCC3-STBY
P3-104	VCC3-STBY
P3-106	VCC3-STBY
P3-108	SPARE
P3-110	GND
P3-112	SPARE
P3-114	PCM-BVD1
P3-116	PCM-VPPEN
P3-118	PCM-CE#
P3-120	AC97-BITCLK
P3-122	GND
P3-124	AC97-RST#
P3-126	LCD-B0
P3-128	LCD-R0
P3-130	LCD-VDDEN
P3-132	CRT-R
P3-134	GND
P3-136	CRT-G
P3-138	TV-OUT
P3-140	CRT-VSYNC

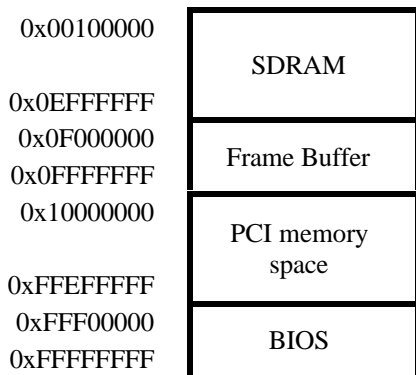
P3-69	LB-DREQ0
P3-71	LB-DACK0#
P3-73	LB-DREQ1
P3-75	LB-DACK1#
P3-77	JTAG-TCK
P3-79	VCORE
P3-81	JTAG-TMS
P3-83	JTAG-TDI
P3-85	JTAG-TDO
P3-87	JTAG-TRST#
P3-89	VIP-D7
P3-91	VCC3-3
P3-93	VIP-ODD/EVEN
P3-95	SLEEP-OUT#
P3-97	SPARE
P3-99	VCC5-STBY
P3-101	SPARE
P3-103	VCORE
P3-105	SPARE
P3-107	VCC3-STBY
P3-109	VCC3-STBY
P3-111	VCC3-STBY
P3-113	PCM-BVD2
P3-115	VCORE
P3-117	PCM-VCCEN
P3-119	AC97-SDIN0
P3-121	AC97-SDIN1
P3-123	AC97-SDOUT
P3-125	AC97-SYNC
P3-127	VCC3-3
P3-129	CRT-HSYNC
P3-131	VCC5
P3-133	CRT-B
P3-135	VCC3-3
P3-137	USB4-P
P3-139	USB4-N

6. MEMORY and I/O mapping

6.1. Memory space usage in the first 1MB

0000:0 - A000:0	Standard Low memory
A000:0 - C000:0	Graphic Memory Available if graphics controller is not enabled
C000:0 - D000:0	VGA BIOS
D000:0 - E800:0	Used by the NAND Flash Driver under DOS / BIOS
E800:0 - FFFF:F	BIOS

6.2. Memory space usage above first 1MB



The “Frame Buffer” cannot be accessed directly, this address space is left unused in the system

6.3. I/O space Usage

The table below specifies all I/O regions known to be used in standard / legacy PC architecture and regions used by on-board peripheral devices.

Address	Function	Comments
0x000-0x00F	Slave DMA regs	
0x020-0x021	Master Interrupt controller	
0x040-0x043	PIT registers	

CM-iVCF Embedded PC Module

0x04E-0x04F	SIO configuration space	
0x060-0x064	Keyboard / PS2 mouse registers	
0x080	General purpose IO register	
0x081-0x083	DMA controller registers	
0x084-0x086	General purpose IO register	
0x087	DMA controller registers	
0x088	General purpose IO register	
0x089-0x08B	DMA controller registers	
0x08C-0x08F	General purpose IO register	
0x092	System Control Port	
0x0A0-0x0A1	Slave interrupt controller registers	
0x0C0-0x0DF	DMA control regs	
0x1F0-0x1F7	IDE0 controller	
0x290-0x297	Hardware monitor	
0x2F8-0x2FF	COM-B	
0x378-0x37F	Parallel Port (LPT1)	
0x3B0-0x3DF	Legacy VGA base	
0x3E0-0x3E1	PCMCIA / CardBus	
0x3F8-0x3FF	COM-A	
0x3F0-0x3F7	Floppy and alternate IDE0 address.	
0x400-0x403	Parallel port in ECP Mode	
0x800-0x87F	Power management, GPIO control registers (PMIO)	
0xCF8-0xCFF	PCI configuration space access window	
0xFFFF0-0xFFFFF	SMBus controller	

6.4. BIOS Flash Mapping

Starting address in flash window	End address in flash window	Usage
0xFFFF80000	0xFFFFAFFFF	Reserved
0xFFFFB0000	0xFFFFBFFFF	Setup and configuration block
0xFFFFC0000	0xFFFFFFFFFF	BIOS area

Setup and Configuration Block Usage

Addresses	Value / Description
0x0000-0x0001	0xAAAA – the signature that the valid CMOS image is in the flash
0x0002-0x01FF	CMOS image, including RTC

7. Power Consumption

The current consumption measurements specified below were performed on a system with the following configuration:

- CM-iVCF-D256-C1000-N128-E-S-AT-V
- ATX-E-L-V-A-C3-X6-Y2-Z6

Current consumption is specified for the both boards. However, 95% of the total current is consumed by CM-iVCF module.

CPU Clock	Activity	Current from 3.3V	Current from 5.0V
300 MHz	Idle	0.39A	0.94A
	Max load	0.45A	1.4A
667 MHz	Idle	0.39A	1.1A
	Max load	0.45A	2.0A
1000 MHz	Idle	0.39A	1.3A
	Max load	0.45A	2.5A

Minimum power consumption

- Idle
- CPU clock - 300 MHz

$$[3.3V * 0.39A] + [5.0V * 0.94A] = 6 \text{ watt}$$

Maximum power consumption

- CPU clock - 1000 MHz
- Max load

$$[3.3V * 0.45A] + [5.0V * 2.5A] = 14 \text{ watt}$$

8. Performance Benchmarks

Measured with CPU @ 1000 MHz, using SiSoft Sandra bench test under Windows.

Drystone (integer)	1,545 MIPS
Wetstone (floating point)	336 MFLOPS
DDR bandwidth	220MB/s

9. Operating Temperature Ranges

The CM-iVCF is available with three options of operating temperature range:

Range	Temp.	Description
Commercial	0° to 70° C	Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20° to 70° C	Every card is individually tested for the lower limit (-20° C) qualification.
Industrial	-40° to 85° C	Every card is individually tested for both lower and upper limits and at several midpoints.

* Temp - maximum temperature measured on hottest spot of heatsink.

For more information regarding availability of card for Industrial grade, please refer to [Products] >> [Industrial Temperature] links in CompuLab's web-site.

Heat Dissipation

User must assure that heatsink temperature would not exceed allowed maximum. In still air heatsink temperature can rise up to 50°C above ambient. For example, at room temperature of 25°C powered card will reach 75°C.

Heatsink should be cooled by airflow or heat exchangers. Even slight indirect airflow in the case will reduce heatsink temperature by 20-30°C. If no airflow is available, metal case should be used and heatsink should be attached to case wall.